Synthesis Environment Guide

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| --- | --- | --- | --- |
| Date | Version | Comment | Author |
| 2016/10/20 | v1.0 | Initial version | Yi Li |
| 2016/1/14 | V2.0 | Adding formality environment | Yi Li |
| 2017/05/04 | V3.0 | Resetn sdc | Yi Li |

1. **Purpose**

The synthesis environment integrates standard cell library path so that everyone no need to care about the path of each stdcell db.

1. **Location**

The demo syn environment is located in **/home/yli/Sirius/trunk/syn/dc\_env**

The user can copy the whole directory into your own synthesis path.

1. **File Tree**

|  |  |  |  |
| --- | --- | --- | --- |
| ./dc | clean.sh | | clean trash files |
| data\_dc | | dc output file directory |
| data\_dcg | | dcg output file directory |
| def | | .def file input directory |
| logs | | log file directory |
| notes.txt | | doc about synthesis environment |
| rpt\_dc | | dc rprt file directory |
| rpt\_dcg | | dcg rpt file directory |
| scripts | dc\_run.tcl | dc run scripts |
| dcg\_run.tcl | dcg run scripts |
| read\_design.tcl | read design scripts |
| fm\_run.tcl | fm run scripts |
| read\_db.sh | to generate fm.db |
| workdir | readme.txt | doc about how to run scripts |
| run | run scripts |
| user\_define | 0\_lib\_setup | macro db file such as memory IP |
| 1\_design\_setup | top name |
| 2\_rtllist | RTL filelist |
| 3\_constraint | timing constraints |
| 4\_power | Power setting |
| 5\_dft | dft scripts |

1. **Step**

I. Before starting synthesis, please make sure you have modified these files,

1) ./user\_define/0\_lib\_setup     #macro db file such as memory IP.

2) ./user\_define/1\_design\_setupl   #top name

3) ./user\_define/2\_rtllist             #RTL filelist

4) ./user\_define/3\_constraints     #timing constraints

II. When all the files are ready, you can change your path into workdir and implement the synthesis scripts.  The option of run command is illustrated in the table,

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Required | Required | Optional | Optional |
| ./run | dc | -7t | default (lvt + svt) | default (ssg corner) |
| dcg | -9t | -svt (only svt) | -tt (tt corner) |
|  | -12t |  |  |
| fm |  |  |  |

We can use this command as the following examples,

1) ./run dc -7t       #run dc, using 7t track, LVT+SVT stdcell at ssg0p81vn40c

2) ./run dc -9t -svt   #run dc, using 9t track, SVT stdcell at ssg0p81vn40c

3) ./run dcg -12t -tt  #run dcg, using 12t track, LVT+SVT stdcell at tt0p9v85c

4) ./run dc -9t -svt -tt   #run dc, using 9t track, SVT stdcell at tt0p9v85c

5) ./run fm #run formality tool

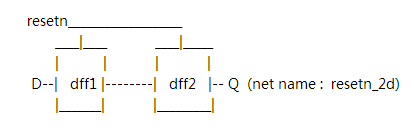
Notes

ssg corner : ssg 0.81v -40c

tt corner : tt 0.9v 85c

1. **Tips**

Asynchronous resetn should be sync implemented as the following circuit architecture,



Please set sdc as below,

set\_false\_path -from [get\_ports resetn]

set\_ideal\_network [get\_pins dff2/Q]

set\_dont\_touch [get\_nets resetn\_2d ]